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Implementation of Area, Delay and Power Efficient Carry-Select Adder

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Abstract: Carry Select Adder (CSLA) is one of the fastest adder which performs fast arithmetic functions in many data processing processors. A conventional CSLA has less carry propagation delay (CPD) than ripple carry adder (RCA). Carry select adder provide compromise between RCA and carry look ahead adder.

For the CSLA new logic is proposed by reducing redundant logic operations present in conventional CSLA. In the proposed scheme the carry select (CS) operation is schedule before calculation of final sum. This is different approach from the conventional. Two carry words (c_{in} = 0 and 1) bit patterns and fixed c_{in} bits is use for generation units and CS logic optimization. Final sum and carry is calculated by using pipelining structure. The proposed work is carried out using Modelsim SE 6.3f and Quatus2 software.

Keywords: Adder, arithmetic unit, low power, CSLA, RCA, low delay, area efficient.

I. INTRODUCTION

In VLSI system design high speed, area and power efficient data path logic systems are the major areas of research. With the increasing the necessity of portable systems, area occupancy plays a vital role in the design of Integrated Circuits. Basic building blocks of any processor or data path application are Adders. The critical path in adder design is carry generation. In arithmetic logic unit and in other parts of the processor adders are used to calculate table, indices addresses and similar applications. In multipliers, high speed integrated circuits and digital signal processing various algorithms like FFT, IIR and FIR are executed by adders. Several adders are involves in complex digital signal processing system. The performance of a complex Digital signal processing system is improved by using an efficient adder design.

There are several types of adder designs available (RCA, CLAA, CSA, CSA). A simple design is used by RCA. The ripple carry adder is made up of cascaded single bit full adders. In ripple carry adder each full adder can only start operation when previous carry out signal is ready so computational speed is slow. Ripple carry adder have compact design but high computation time. Carry look ahead adder have increase in area but gives fast result. Compromise between Carry look ahead adder and RCA is given by Carry select adder. Carry select adder have less area and power consumption. Partial sum and carry is generate by using carry input C_{in}=0 and C_{in}=1 and the final sum and carry are selected by using the multiplexers. In digital adders the time required by the carry to propagate through the adder limits the speed of addition.

II. LITERATURE SURVEY

The largest systems in VLSI system design are design of low delay, area and power. Different researchers have done work on this and few are summarised below

M.chithra and G.omkareswari [2] proposed that a simple approach to reduce the area and power of CSLA architecture. RCA is used to implement a carry select adder (CSLA). By comparison with the regular 128-bit CSLA the proposed design 128-bit CSLA has reduced more delay and area. This work offers advantage in the reduction of area and total power by reducing number of gates. The modified CSLA architecture is low area, low power, simple and efficient for VLSI hardware implementation.

Pandu Ranga Rao and Priyanka Halle [3] proposed that use of a simple and an efficient gate level modification reduces area and delay of the CSLA. By using this concept 16, 32, 64 and 128 bit SQRT CSLA is improved. Area and delay of proposed design is reduced when compared with the regular SQRT CSLA. Replace the RCA with BEC in the structure reduces the number of gates. In modified SQRT CSLA the delay is reduced to a great extent.

Damarla Paradhasaradhi and Prof. K.Anusudha [4] proposed that an area efficient carry select adder by sharing the common Boolean logic term (CBL). The correct output is selected according to the logic states of the carry in signal through the multiplexer. Based on this modification a new architecture has been developed using Binary to Excess-1 converter (BEC). The proposed architecture has reduced area and delay when compared with the regular SQRT CSLA architecture. An 8-bit inputs area efficient square-root carry select adder is proposed. The reduced number of gates gives advantage in the reduction of area.

Sajesh Kumar U and Mohamed Salih K K [6] proposed the carry select adder configuration and parallel adder approach for the implementation of fast adder for the efficient implementation of parallel adder with optimized area and propagation delay for FPGA applications.

III. PROPOSED WORK

An RCA–RCA configuration is used in a conventional carry select adder (CSLA) and a pair of output carry bit and sum words bit is generated. The Carry Select Adder comes in the category of conditional sum adder. Conditional sum adder works on some condition.

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CSLA have a lesser delay than Ripple Carry Adders. Carry Select Adder is used while working with smaller number of bits. Different logic formulation is used to reduce delay and area so that speed is increased. The expressions of full adder are listed below

$$SUM=A \text{ xor } B \text{ xor } C \quad (1)$$

$$CARRY = (A.B) + (B.C) + (C.A) \quad (2)$$

Fig.1 shows Internal architecture of 4 bit CSLA. Two ripple carry adders are multiplexed together. Sum and carry are calculated by assuming input carry as 1 and 0 prior the input carry comes. When actual carry input arrives, the actual calculated values of sum and carry are selected using a multiplexer. Behavioral modeling is used for code.

Fig.2 shows basic building block of a CSLA of block size 4. A ripple carry adder layout is simple. C_{out} is the output carry and s0, s1, s2, s3 are the sum produce. Structural modeling is used for code.

Fig.3 shows 4 bit CSLA where c0 and 4 bit a and b input is applied. s0, s1, s2, s3 are the sum produce by using adder and c4 is output carry produce. Mixed modeling is used for code.

Fig.4 shows BEC based CSLA. In BEC circuit 1 is added to input numbers. Final sum and final carry is calculated from sum and carry selection unit

Fig.5 shows 4 bit Binary to Excess-1 Convertor. The expressions of 4 bit BEC are listed below.

$$X0=\sim B0 \quad (3)$$

$$X1=B0 \wedge B1 \quad (4)$$

$$X2=B2 \wedge (B0\&B1) \quad (5)$$

$$X3=B3 \wedge (B0\&B1\&B2) \quad (6)$$

Fig.6 shows CBL based CSLA. By sharing the common Boolean logic term duplicated adder cells in the conventional CSLA can remove.

Fig.7 shows Proposed CSLA before calculation of final sum CS operation is schedule and pipelining structure is used to calculate final sum and final carry.

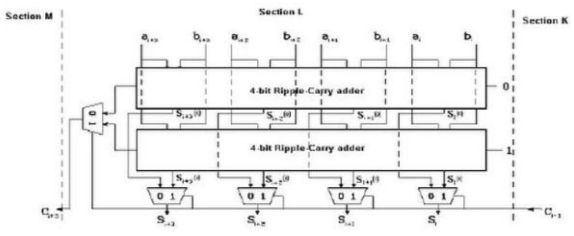

Fig.1 Conventional CSLA

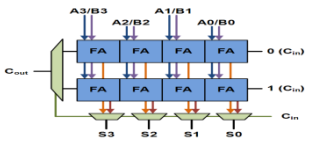

Fig.2 Basic block of a CSLA of size 4

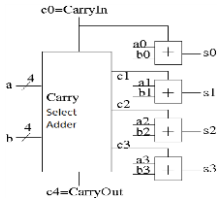

Fig.3 4 bit CSLA

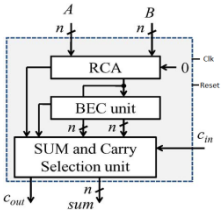

Fig.4 BEC Based CSLA

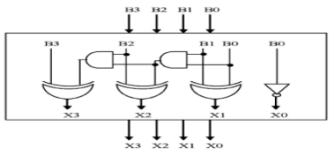

Fig.5 4 bit Binary to Excess-1 Convertor

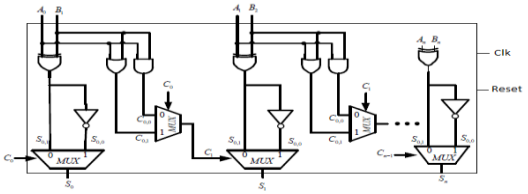

Fig.6 CBL Based CSLA

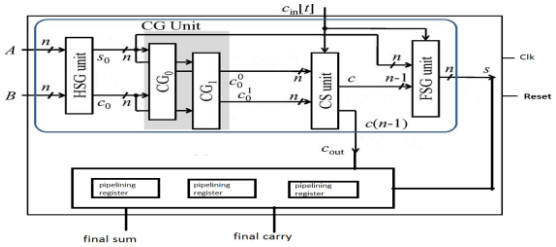

Fig.7 Proposed CSLA

IV. RESULT

The area analysis, time analysis and power analysis for conventional CSLA, basic building blocks of CSLA of size 4, 4 bit CSLA, BEC based CSLA, CBL based CSLA and Proposed CSLA is shown in following figures.

Flow Status	Successful - Sat Mar 21 19:07:12 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa
Top-level Entity Name	csa
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	7 / 18,752 (< 1 %)
Total combinational functions	7 / 18,752 (< 1 %)
Dedicated logic registers	0 / 18,752 (0 %)
Total registers	0
Total pins	20 / 315 (6 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.8 Area analysis for the Conventional CSLA

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Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	13.439 ns	x3[0]	y1[0]	--	--	0
2	Total number of failed paths								0

Fig.9 Time analysis for Conventional CSLA

PowerPlay Power Analyzer Status	Successful - Sat Mar 21 19:05:14 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa
Top-level Entity Name	csa
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	69.01 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	21.66 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.10 Power analysis for Conventional CSLA

Flow Status	Successful - Sat Mar 21 20:00:28 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa2
Top-level Entity Name	csa2
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	13 / 18,752 (< 1 %)
Total combinational functions	13 / 18,752 (< 1 %)
Dedicated logic registers	0 / 18,752 (0 %)
Total registers	0
Total pins	14 / 315 (4 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.11 Area analysis for the for basic block of a CSLA of size 4

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	14.169 ns	carry	outsum[3]	--	--	0
2	Total number of failed paths								0

Fig.12 Time analysis for basic block of a CSLA of size 4

PowerPlay Power Analyzer Status	Successful - Sat Mar 21 20:02:15 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa2
Top-level Entity Name	csa2
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.33 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	20.98 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.13 Power analysis for basic block of a CSLA of size 4

Flow Status	Successful - Sat Mar 21 20:14:59 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	carry_select_adder
Top-level Entity Name	carry_select_adder
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	9 / 18,752 (< 1 %)
Total combinational functions	9 / 18,752 (< 1 %)
Dedicated logic registers	0 / 18,752 (0 %)
Total registers	0
Total pins	14 / 315 (4 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.14 Area analysis for 4 bit CSLA

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tpd	N/A	None	14.695 ns	y[2]	z[3]	--	--	0
2	Total number of failed paths								0

Fig.15 Time analysis for 4 bit CSLA

PowerPlay Power Analyzer Status	Successful - Sat Mar 21 20:21:09 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	carry_select_adder
Top-level Entity Name	carry_select_adder
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.33 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	20.98 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.16 Power analysis for 4 bit CSLA

Flow Status	Successful - Sun Jun 21 13:56:36 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa4
Top-level Entity Name	csa4
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	13 / 18,752 (< 1 %)
Total combinational functions	13 / 18,752 (< 1 %)
Dedicated logic registers	8 / 18,752 (< 1 %)
Total registers	8
Total pins	16 / 315 (5 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.17 Area analysis for BEC based CSLA

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	5.630 ns	b[0]	temp1[3]	--	clk	0
2	Worst-case tco	N/A	None	7.950 ns	temp1[3]	outcarry	clk	--	0
3	Worst-case tpd	N/A	None	12.348 ns	b[0]	outcarry	--	--	0
4	Worst-case th	N/A	None	-3.296 ns	carry	temp1[0]	--	clk	0
5	Clock Setup: 'clk'	N/A	None	Restricted to 380.08 MHz (period = 2.631 ns)	temp1[2]	temp2[3]	clk	clk	0
6	Total number of failed paths								0

Fig.18 Time analysis for BEC based CSLA

PowerPlay Power Analyzer Status	Successful - Sun Jun 21 13:55:17 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa4
Top-level Entity Name	csa4
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.55 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	21.20 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.19 Power analysis for BEC based CSLA

Flow Status	Successful - Sun Jun 21 13:59:10 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa_cbl
Top-level Entity Name	csa_cbl
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	5 / 18,752 (< 1 %)
Total combinational functions	5 / 18,752 (< 1 %)
Dedicated logic registers	5 / 18,752 (< 1 %)
Total registers	5
Total pins	16 / 315 (5 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.20 Area analysis for CBL based CSLA

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	4.813 ns	a[1]	temp4[1]	--	clk	0
2	Worst-case tco	N/A	None	8.012 ns	temp4[3]	outsum[3]	clk	--	0
3	Worst-case th	N/A	None	-2.822 ns	b[2]	temp4[2]	--	clk	0
4	Total number of failed paths								0

Fig.21 Time analysis for CBL based CSLA

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PowerPlay Power Analyzer Status	Successful - Sun Jun 21 14:00:34 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa_cbl
Top-level Entity Name	csa_cbl
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.55 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	21.20 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.22 Power analysis for CBL based CSLA

Flow Status	Successful - Tue May 12 22:24:27 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa_proposed
Top-level Entity Name	csa_proposed
Family	Cyclone II
Device	EP2C20F484C7
Timing Models	Final
Met timing requirements	Yes
Total logic elements	13 / 18,752 (< 1 %)
Total combinational functions	13 / 18,752 (< 1 %)
Dedicated logic registers	5 / 18,752 (< 1 %)
Total registers	5
Total pins	16 / 315 (5 %)
Total virtual pins	0
Total memory bits	0 / 239,616 (0 %)
Embedded Multiplier 9-bit elements	0 / 52 (0 %)
Total PLLs	0 / 4 (0 %)

Fig.23 Area analysis of proposed CSLA

Timing Analyzer Summary

	Type	Slack	Required Time	Actual Time	From	To	From Clock	To Clock	Failed Paths
1	Worst-case tsu	N/A	None	6.946 ns	a[1]	temp4[3]	--	clk	0
2	Worst-case tco	N/A	None	7.438 ns	temp3	outcarry	clk	--	0
3	Worst-case th	N/A	None	-3.043 ns	carry	temp4[1]	--	clk	0
4	Total number of failed paths								0

Fig.24 Time analysis of proposed CSLA

PowerPlay Power Analyzer Status	Successful - Tue May 12 22:26:49 2015
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	csa_proposed
Top-level Entity Name	csa_proposed
Family	Cyclone II
Device	EP2C20F484C7
Power Models	Final
Total Thermal Power Dissipation	68.54 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	47.35 mW
I/O Thermal Power Dissipation	21.19 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

Fig.25 Power analysis of proposed CSLA

Table. 1 Comparison of Adders for Area, Delay and power

Adder	Area (total pins)	Delay (ns)	Power(mW)
BEC based CSLA	16/315 (5%)	7.950	68.55
CBL based CSLA	16/315 (5%)	8.012	68.55
Proposed CSLA	16/315 (5%)	7.438	68.54

V. CONCLUSION

Power, delay and area are the important factors that determine the performance of any circuit in VLSI design process. The disadvantage of regular CSLA is more power consumption and large area. The reduced number of gates offers the advantage in the reduction of area and total power. The proposed CSLA have less delay and power than BEC Based CSLA and CBL based CSLA.

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